CIRCUIT DESIGNER'S NOTEBOOK

Capacitors in Bypass Applications

Capacitors used in bypass applications are implemented as shunt elements and serve to carry RF energy from a specific point in the circuit to ground. Proper selection of a bypass capacitor will provide a very low impedance path to ground. In theory the ideal impedance is zero ohms; however a real capacitor will exhibit some impedance due to its reactance and inherent parasitic elements. Satisfying capacitive bypass application requirements entails careful analysis of various frequency dependent capacitor parameters such as series resonant frequency (F_{SR}), equivalent series resistance (ESR), and the magnitude of the impedance. The ESR and impedance should always be evaluated at the operating frequency.

Figure 1 is a block diagram illustrating a capacitor bypass application. Capacitor C_0 in this figure is represented with its equivalent series resistance denoted as R_S, equivalent series inductance (ESL) denoted as L_S and parasitic parallel capacitance C_P, associated with the parallel resonant frequency (F_{PR}).

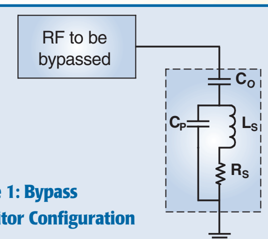

Figure 1: Bypass Capacitor Configuration

Terminology:

Equivalent Series Resistance (ESR): Is the summation of all losses resulting from the dielectric (R_{SD}) and metal elements (R_{SM}) of a capacitor (R_{SD} + R_{SM}) and is typically expressed as milli-ohms. R_{SD} is the dielectric loss tangent and is dependent upon specific characteristics of the dielectric formulation and processing. Metal losses are dependent on resistive characteristics of the electrode and termination materials, as well as the losses of the electrodes due to skin effect. ESR is a key parameter to consider when utilizing capacitors in RF bypass applications.

Quality factor (Q): A capacitor's Q is numerically equal to the ratio of its net reactance (X_C - X_L) to its equivalent series resistance (ESR) or $Q = |X_C - X_L| / ESR$. From this expression it can be seen that the capacitor's Q varies inversely to its ESR and directly with its net reactance.

Series Resonant Frequency (F_{SR}): A resonance that occurs at $F_{SR} = 1/2\Pi\sqrt{L_S C_O}$. At this frequency the capacitor's net reactance is zero and the impedance is equal to the ESR. The capacitor will provide its lowest impedance path required for optimal bypassing at this frequency.

Parallel Resonant Frequency (F_{PR}): A resonance occurring at approximately twice the F_{SR} for a parallel plate capacitor. In contrast to F_{SR} the impedance of a capacitor at its F_{PR} can be precipitously high. This is readily observed by assessing the magnitude of the insertion loss at F_{PR}.

Impedance: (Z) The magnitude of a capacitor's impedance is equal to $\sqrt{(ESR)^2 + (X_L - X_C)^2}$. As seen by this relationship a capacitor's impedance is significantly influenced by its net reactance (X_L-X_C).

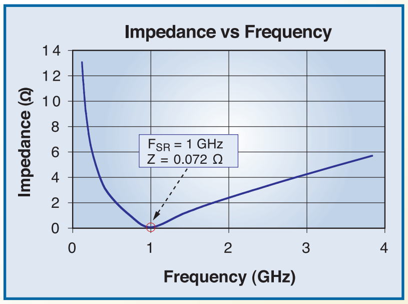

Figure 2: Impedance vs. Frequency for ATC100A101 (100pF)

It is important to evaluate the magnitude of the impedance throughout the desired frequency range. A properly selected bypass capacitor will exhibit suitably low impedance over this range. As seen in Figure 2 the net impedance below F_{SR} is capacitive and is dominated by $1/\omega C$, yielding a hyperbolic curve for frequencies less than F_{SR}. Conversely, the net impedance above F_{SR} is inductive and is dominated by ωL yielding a linear line segment for frequencies greater than F_{SR}.

Application Example

Bypassing is a critical design matter that requires careful consideration. Figure 3 shows a 1.9 GHz cellular FET amplifier with emphasis on the drain bias network.

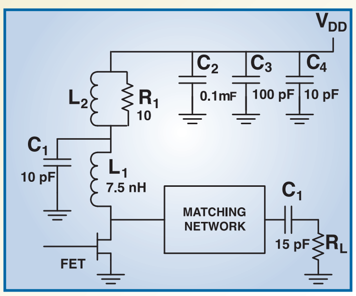

Figure 3: Bypass Capacitors in a 1.9GHz FET Broadband Bias Network

The circuit elements depicted in this figure will serve to suppress RF energy from getting onto the V_{DD} supply line while providing high impedance at the drain in order to maintain optimum in-band RF gain. It also functions to keep noise generated by the power supply from appearing on the drain of the FET. High-speed switching environments created by switch mode power supplies (SMPS) will generate noise on V_{DD} supply lines. Instantaneous current generated by fast rising and falling switch pulse edges can easily cause the V_{DD} supply line to ring. The resultant noise can include frequencies of up to several hundred megahertz. RF noise generated by SMPS switching is continuous and will generally occur up to frequencies equal to $0.35 / P_E$, where P_E = pulse rise or fall time (sec). For example a switched pulse with a rise and fall time of 1.5 ns will yield spurious spectral components up to 233 MHz.

Drain Bias Network:

As illustrated in figure 3, the FET's drain bias network consists of series inductive elements having an impedance of ωL and shunt capacitive elements with an impedance of $1/\omega C$. Proper selection of bypass capacitors in the bias network is essential as they will serve to de-couple RF energy from the V_{DD} supply line to ground over a wide range of frequencies.

Since capacitors exhibit a small parasitic inductance there is an associated series (self) resonant frequency where $F_{SR} = 1/2\Pi\sqrt{L_S C_O}$. At F_{SR} the magnitude of the inductive and capacitive reactances are equal and hence the net impedance $\sqrt{(ESR)^2 + (X_L - X_C)^2}$ is equal to a small ESR value. Accordingly the designer will ideally select a capacitor that has an F_{SR} at or close to the desired "bypass frequency". This preference is based on establishing a low impedance path with minimal or zero net reactance thereby making it ideal for bypassing applications.

F_{PR} usually occurs at more than twice F_{SR} for most multi-layer ceramic capacitors. At the capacitor's F_{PR}, the impedance is likely to be high and inductive ($R + j\,\omega L$) and may not provide an adequate RF path to ground. To alleviate this, several capacitors are selected such that their self-resonant frequencies are staggered in order to cover a wide range of frequencies with reasonably low loss. The number of required capacitive elements depends on the loss and impedance characteristics of each element over the intended frequency band segments.

The inductors are in series with the drain and are not directly connected to reference RF ground. Accordingly they rely on bypass capacitors, C_1 through C_4 to achieve a low impedance path to ground. The combination of L_1 and C_1 will greatly suppress the in-band 1.9 GHz carrier frequency energy from appearing on the V_{DD} supply line. Inductor L_1 will act as a block at this frequency while capacitor C_1 will serve to further suppress in-band RF energy by bypassing it to ground. L_2 C_2, C_3 and C_4 will suppress RF energy at frequencies below the 1.9 GHz carrier frequency where the gain of the amplifier may be much higher. C_1's capacitance value is selected such that its F_{SR} is close to the amplifiers operating frequency. Since C_1 is a shunt element, and the impedance is low at its F_{SR}, the RF energy at the operating frequency will be bypassed to ground. Capacitor elements C_2, C_3 and C_4 are staggered in value and selected so that the impedance of each will be low at successive frequency segments in order to offer continuous bypassing of frequencies below the amplifier's operating band.

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