

ATC Resistors and Terminations: Engineering Guidelines

Design, Test and Measurement, Performance and Mounting

Both resistors and terminations are available in several different package styles. Those shown in Figs. 1 and 2 are meant to be mounted (usually by soldering) to a metallic ground plane, either in a cutout in a microstrip board or adjacent to a board edge (see Figure 3a). The contact area on the chip has a silver tab parallel-gap welded to it; the free end of the tab is soldered to the microstrip trace. Heat generated in the resistive film is conducted by the chip substrate to the ground plane. Other configurations are designed to avoid the necessity of a cutout or proximity to a board edge; these are so-called surface mount parts and are typically soldered to a via-patch on the PC board's top surface. The via patch transfers the generated heat to the ground plane (see Figure 3b). A schematic overview of the various chip configurations and their designations is shown in Figure 4. Note that the CW style has no ground conductor; heat from the resistive film can be removed only through the end contacts, by convection, or by radiation. In practice, all resistive films are covered with a thin layer of a special epoxy that helps protect against solvents, moisture, handling, and other environmental hazards. Other packaging options (not shown) include ceramic covers for additional environmental protection and marking, and flange mounts that enable parts to be screwed down to mounting surfaces rather than soldered.

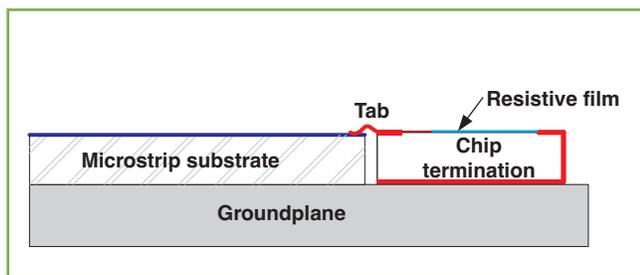


Figure 3a: Groundplane-mounted chip

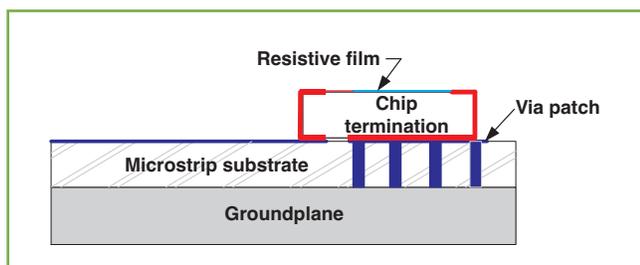


Figure 3b: Surface-mounted chip

SPECS AND SPECMANSHIP

The thermal and electrical properties of resistive chips are intimately related, and very often can be traded off against one another. Among those important to end-users are:

- (1) Resistance change over time (long term)
- (2) Maximum temperature reached by the resistive film
- (3) Resistance change with temperature (short term)
- (4) Resistance change with applied voltage (short term)
- (5) Reflection magnitude (VSWR) vs. frequency (terminations) or capacitance (resistors)

Property (1), variously termed "aging" or "stability" or "life," refers to a change in the value of resistance that typically occurs

over hundreds or thousands of hours of operation. It depends on the temperature reached by the film (which, among many factors, in turn depends on the properties of the mounting surface) and may depend on applied voltage as well. Property (2) may affect the lifetime or behavior of other devices in proximity to the resistive chip. Properties (3) and (4) are generally short-term – e.g. change occurs over a few minutes – measures of stability, usually presented as TCR, the Temperature Coefficient of Resistance and VCR, the Voltage Coefficient of Resistance. Property (5) is a fundamental measure of electrical performance needed for operation of the circuit or sub-system in which the resistive chip is used.

Resistive chip design must simultaneously consider properties (1) through (5), because of the tradeoffs involved. In practice, two problems arise, usually with (1), (2), and (5): End-users fail to precisely define the measurement conditions and vendors do likewise with their specifications.

- Vendor power ratings, for example, are usually given for parts mounted on "an ideal heat sink," or "an infinite heat sink" without explanation as to how a user can de-rate the part for operation on a real heat sink – or, for that matter, how the vendor arrived at the rating in the first place.
- It will be shown that temperatures vary along both film and mounting surfaces, yet virtually no one states exactly at what point the mounting surface temperature was, or ought to be, measured.
- Devices with ceramic covers make end-user film temperature measurements impossible.
- End-users are most often concerned about aging with RF power applied, whereas vendors typically use DC in their testing – and, in general, it makes a difference.

	<u>Style</u>	<u>Device</u>
	CZ	termination
	CT	termination
	CR	resistor
	CS	resistor
	CW	resistor

Figure 4: Resistor and termination styles

- End-users may specify VSWR, but not precisely define the interface between the resistive device and their board, e.g., Is the board thicker or thinner than a termination's substrate? Is the user's trace wider or narrower than the termination's tab? What is the substrate dielectric constant? Is the tab being bent to provide strain relief? Etcetera. All of the above affect the actual VSWR that the user will measure. And vendors are often equally vague about the test conditions under which they determined the device's specifications.

In an informal survey of large-volume users of resistive devices, the following comments were made when respondents were asked what criteria they used to evaluate vendor claims about the supplied product:

"We do no incoming inspection. We just put it in our system, blast it with power, and see if it survives. Beyond that, we just rely on manufacturers' test data."

"Regardless of vendor, we operate at a maximum of half their claimed power rating. Vendors almost never say what the maximum film temperature should be. For measurements on flanged parts, we put a thermocouple on top of the flange, as near to the part as possible."

"We are more interested in maximum film temperature than aging. We verify the film temperature using thermal imaging [camera]. We will sometimes ask the vendor for de-capped parts. We locate our mounting-surface thermocouple at some point away from the device."

"We locate our ambient-temperature thermocouple under the part underneath the heat sink. We apply the maximum rated RF power for several thousand hours and check the temperature with an IR scanner. Failure is defined as aging beyond the specified tolerance at room temperature."

The vagueness and lack of consistency in user requirements and test methods makes it difficult for a meticulous supplier to decide on rational design and test criteria, and correspondingly makes it easier for less meticulous vendors to specify and furnish their product. As a member of the meticulous supplier group, ATC has attempted to evolve a set of logical design steps and precisely defined test methodologies that will facilitate customer evaluation of our products.

DESIGN STEPS: A SUMMARY

- Select a thin- or thick-film implementation of the resistor and specific materials.
- Determine the aging characteristics of the film at various temperatures and applied voltages.
- For a given design, determine whether temperature or voltage will be the limiting factor in aging. Note that the two effects may be interactive: Voltage aging may have a temperature dependency.
- If film temperature must be held below a certain value with a specified maximum applied power, determine, with the known properties of the substrate, the minimum film area needed to achieve this. For resistors, this will also determine the film capacitance to the ground plane.
- Determine the film dimensions and impedance matching structure needed to achieve the specified reflection or capacitance.
- Perform design iterations as necessary to accommodate the many practical product constraints, e.g., overall chip size, space required for tab contact, need for a ceramic cover, film dimensional changes

resulting from trimming operations, etc.

Because of our extensive background in thin-film materials and processes and the many advantages of thin-films in the areas of uniformity, reliability, and tight-tolerance capability, ATC has chosen this implementation for its initial group of resistive products. We will proceed with a discussion of design steps B. through F. above; the motive here is to acquaint the reader with some of the tradeoffs involved so that one can determine what is and is not achievable and what specifications may be important in operational use. Test methodologies will be discussed in separate sections.

AGING OF TANTALUM NITRIDE THIN FILMS Oven Aging

Figure 5 shows the average measured change in resistance of four groups of ten each Ta₂N thin-film resistors placed in an oven – no applied power to the resistors – and aged for 1000 hours. The latter number of hours appears to be a de facto industry specification, although the governing military spec, MIL-PRF-55342 calls out 2000 hours. Measurements were made at two different temperatures and were repeated on AIN supplied by different vendors (not shown), and on substrates from the same vendor but having different average surface roughnesses. In general, resistance change during aging, $\Delta R/R$ when expressed as a percentage of initial resistance, followed the formula predicted by theory,¹

$$\frac{\Delta R}{R} = \frac{AR_s}{50} \left(\frac{t}{t_0} \right)^n \exp \left(\frac{-T_0}{T} \right) \quad (1)$$

where

t = time

t₀ = a characteristic time that depends on film material

T = film temperature

T₀ = a characteristic temperature of the material

R_s = sheet resistance

A = a constant dependent on the method of anodization

n = exponent determined by temperature range

There are a few features to note about the plots and about Ta₂N resistive films in general:

- The aging mechanism due to heat is caused by oxidation of the film; the oxide layer begins at the surface exposed to the air, deepens with time and temperature, and forms a tough protective barrier.
- Thinner films, i.e., ones with higher surface resistivities, age more quickly than thicker films, since a larger percentage of their thickness will oxidize.
- Surface roughness affects aging; the lower the roughness, the less the aging. Since polished substrates are more expensive than lapped or as-fired substrates, there is a cost-performance tradeoff.
- From the tests on substrates made by different manufacturers, it was found that unknown surface properties other than average roughness affect aging; different brands having identical surface roughnesses produced different aging. This may relate to the fundamental conduction mechanism postulated for Ta₂N films: substrate-assisted tunneling – and properties such as grain size, grain agglomeration, and impurities.

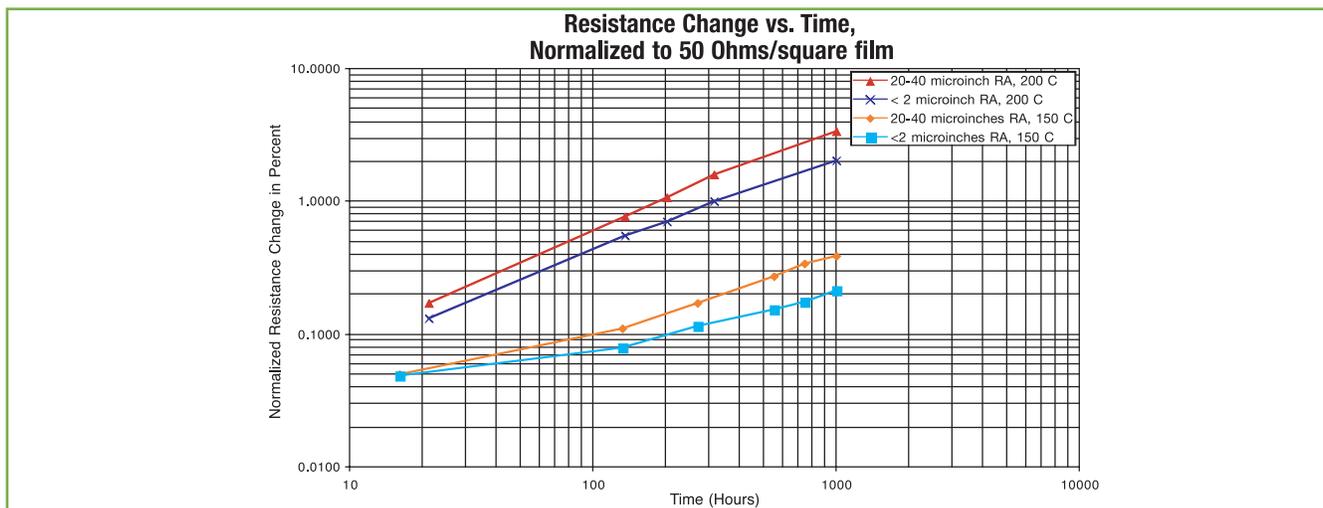


Figure 5: Normalized percent resistance change of TaN oven-aged resistors

The question may now be asked, is aging under powered conditions the same as oven aging? We have already alluded to the possibility of an aging effect with applied DC voltage, but what about AC? The answer is that AC power aging and oven aging tests have shown that current flow in the resistor does not appear to contribute to the change of resistance other than by raising the temperature of the film through the dissipation of heat.

Aging with applied AC power

Figure 6 shows the average measured change in resistance of four 100-ohm, 60-Watt resistors selected at random from a production run and 60-cycle-AC power-aged for 907 hours. The test was done in accordance with MIL-PRF-55342, which requires power to be applied for 90-minute intervals alternating with power-off periods of 30 minutes – except that the Mil spec requires DC instead of AC. In order to magnify changes, sufficient power was applied to heat the resistive films to peak temperatures of about 190 °C; this required about 100 watts, well in excess of the 60-watt maximum rating.

The top curve shows the raw data; average resistance change was about 4.9%. The lower curve shows the data normalized to a 50-ohms/square resistivity, i.e., the resistance change was scaled

by the ratio of actual film resistivity, 72 ohms/square, to 50 ohms/square using equation (1). Since the substrate used had an average surface roughness of 20-40 microinches, the lower curve should be comparable to the 200 °C oven-aged result for this substrate shown in Figure 5. The results are indeed close; oven aging (1000 hours, 200 °C) produced a 3.4% change, AC power aging (907 hours, 190 °C, peak) produced a 3.4% change. This good agreement, however, is somewhat misleading. In addition to the slightly different test times, there are uncertainties connected with the production resistors that make the exact comparison less accurate: (1) Their area-average temperatures were less than the peak temperatures; (2) their exact surface roughness had a range of 20 microinches; and 3) their widths were laser trimmed by amounts ranging from 0 – 20%.

We can conclude this from the experiments: Both oven aging and AC power aging cause resistance to increase with time; if the respective average film temperatures are fairly close, the percentage resistance increases are likely also to be close. It should be noted that when the production resistors are operated at their maximum rated power of 60 watts, they will age much less than they did at the 100 watt level.

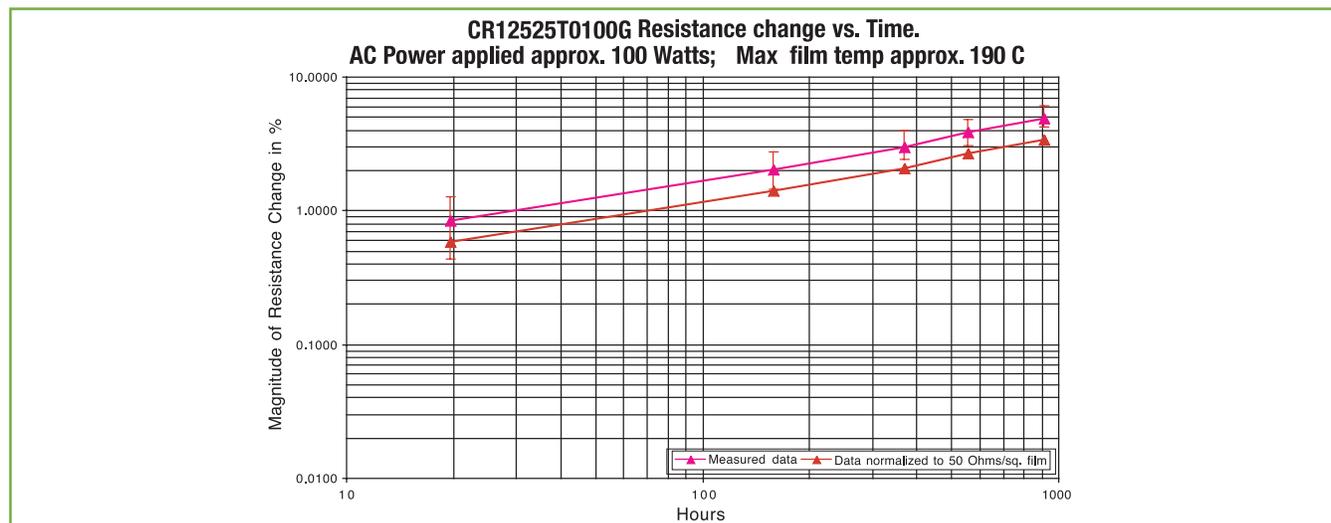


Figure 6: Percent resistance change of TaN resistors with applied 60-cycle AC power

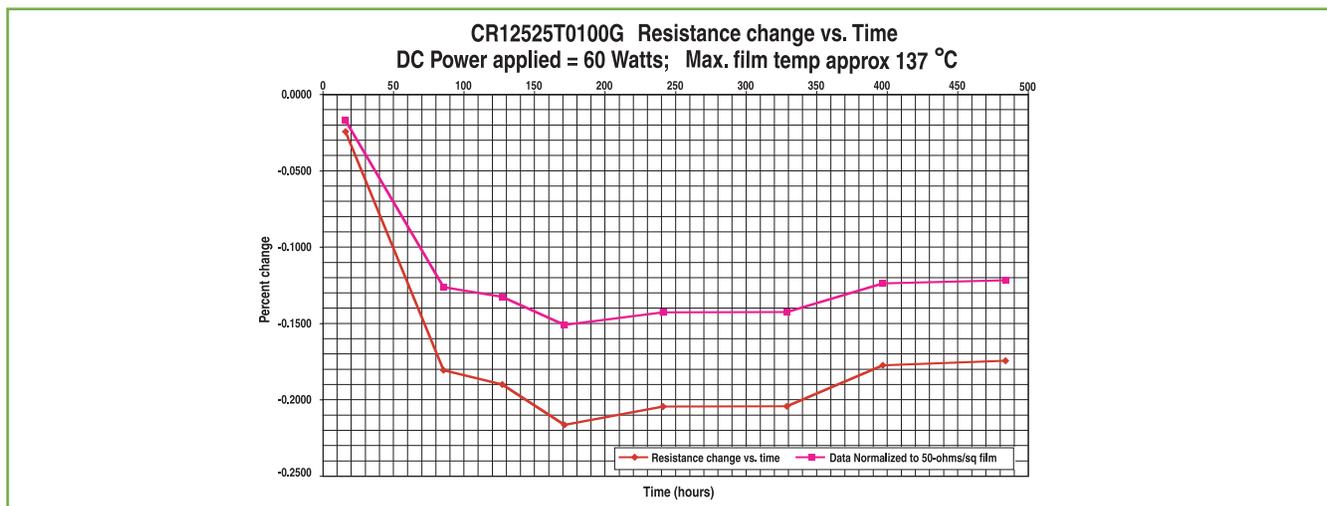


Figure 7: Percent resistance change of TaN resistors with applied DC power

Aging with applied DC power

What now of aging effects due to the application of a DC voltage? **Figure 7** shows the average measured change in resistance of three 100-ohm, 60-Watt resistors selected at random from a production run and DC power-aged – this time exactly in accordance with MIL-PRF-55342 – for 490 hours. The top curve shows the raw data; maximum resistance change was about -0.22% . The lower curve shows the data normalized to a 50-ohms/square resistivity, i.e., the resistance change was scaled by the ratio of actual film resistivity, 72 ohms/square, to 50 ohms/square using equation (1). The meaning of the scaling here is ambiguous, since resistance change is now seen to occur as a result of two separate effects: Heating – to which resistivity scaling applies by virtue of (1) – and a DC voltage sensitivity resulting from unknown causes. The latter phenomenon is common in thick films and is believed to result from an agglomeration of small conductive particles, under the application of a DC potential, into lower resistance larger particles. However, a corresponding thin-film mechanism does not seem to be reported in the available literature. Nevertheless, ATC has observed it experimentally on substrates from a number of different vendors and having a variety of surface roughnesses. The salient feature is that this effect causes resistance to decrease with time, whereas thermal effects cause it to increase. We can infer from Fig. 7 that the DC aging effect dominates for the first 170 hours, after which the thermal effect becomes significant. The fact that the two phenomena yield resistance departures in opposite directions helps to generate good results on the Mil spec test – although it must be cautioned that AC-only use could produce greater changes. Absent specific knowledge of customer use, ATC performs its standard aging test with DC applied per the Mil spec.

FUNDAMENTAL ELECTRO-THERMAL PERFORMANCE LIMITATIONS

Power handling vs. resistor capacitance-to-ground

Assuming, from the aging tests, that the designer now knows the maximum film temperature allowable at full applied power, it must now be determined how to insure it is not exceeded – and what limitations it imposes on electrical performance. **Figure 8** shows the heat flux in a chip termination. We begin with three simplifications to establish an elementary thermal model:

(1) The heat is generated uniformly everywhere in the film; (2) the heat flow is one-dimensional – no spreading – from the film to the bottom of the chip, which is assumed at ambient (thermal ground); and (3) there is no convective or radiative heat flow. Concerning (1), we know that the currents in the film tend to be edge concentrated – much more so the lower the resistivity – and so there will be more heat generated at the edges than at the center. Nevertheless, we expect the approximation to be quite good for film geometries where the length and width are substantially greater than the substrate thickness and for the range of film resistivities typically encountered in RF applications. Additionally, we are not considering tapers, wherein the width of the film and hence the power dissipated at any cross-section may vary along its length. Concerning (2), it is understood that there is indeed thermal spreading, not only from the front face of the film – heat flow lines shown dotted in **Figure 8** – but from the lateral edges as well. Thus, the second and third assumptions are thermally conservative – there will be additional heat paths beyond those accounted for – while the first will need further investigation since edge-located hot spots could develop at RF that would not be revealed in DC tests.

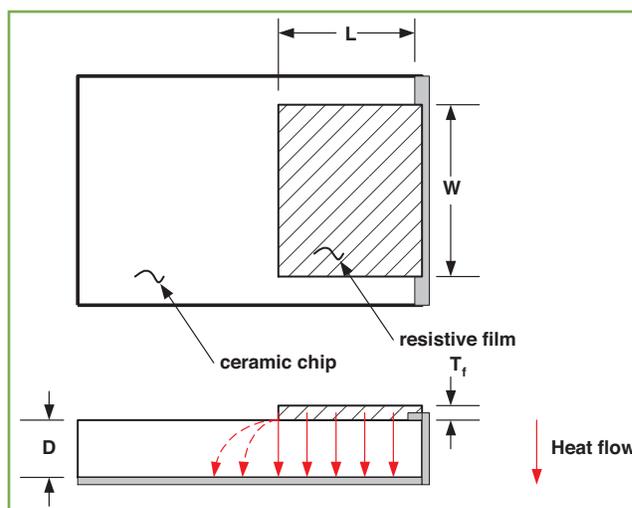


Figure 8: Chip termination showing heat flux

MEASUREMENT AND PERFORMANCE OF CHIP RESISTORS AND TERMINATIONS

The basic formula for one-dimensional steady state heat flow is given as:

$$T - T_A = \Delta T = \frac{P D}{kA} \quad (2)$$

where

T = Temperature of film (°C)
 T_A = Ambient temperature (°C)
 P = Power dissipated in film (Watts)
 D = Substrate thickness (meters)
 A = Area of film (square meters)
 k = Thermal conductivity (Watts/m °C)

Let us consider a practical example: We will assume an ambient temperature, T_A , of 50 °C. We further assume a 40-mil chip thickness – for mechanical strength and substrate availability at moderate price – and seek to limit the maximum film temperature to 150 °C. Using the thermal conductivity of AlN at 200 °C (see Table 1), and setting $P = 20$ watts, we find from (2) that to limit T to 150 °C max. (100 °C above specified ambient) requires a film area of 2624 mils². For $P = 200$ watts, the film area is 26,240 mils².

We next examine what conditions insure that our film behaves as a constant resistance through the highest operating frequency. As is well known, skin effect causes currents to decrease inside conductors, thereby increasing their effective resistance as frequency increases. For a flat plane conductor of finite thickness, D , it may be shown² that if the conductor thickness is 1/2 the skin depth, the conductor will have virtually the same resistance as its DC value. Skin depth (m.) is given by,

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad (3)$$

where

ρ = resistivity of film (ohm-m.)
 f = frequency in Hertz
 μ = permittivity of film (henry/m.)

As noted for thick-film implementations, T_f , the film thickness, is typically on the order of 0.5 mils. If we set $\delta = 2T_f = 1.0$ mils = 2.54×10^{-5} m., we may solve (3) for ρ at the highest operating frequency, F_{hi} . Let us choose $F_{hi} = 6.0$ GHz. The result is that values of $\rho \geq 15.3 \times 10^{-6}$ ohm-m. yield skin depths ≥ 1.0 mil.

The low frequency resistance (ohms) of the film is given by,

$$R_L = \frac{\rho L}{WD_f} \quad (4)$$

where

L = film length (m.)
 W = film width (m.)
 D_f = film thickness (m.)

For a 0.5 mil thick square film, this corresponds to $R_L \geq 1.5$ ohms/square. Since film pastes are readily available in resistivity values ranging from 10 to 1000 ohms/sq., this does not pose severe limitations for most present applications. It may also be seen that thin-film implementations, which typically have film thick-

nesses ranging from 450 – 2250 Angstroms, will clearly not exhibit any significant skin effects up to much higher frequencies than thick films.

In our example, we assumed a 40-mil thick substrate; we may now ask what would be the consequences if we'd chosen another value. Equation (2), after all, indicates that with thinner substrates the temperature rise would be less. The consequences are revealed, however, when we write the expression for (one dimensional, i.e., no electrical fringing fields) film capacitance to the ground plane:

$$C_g = 8.85 \frac{A \epsilon}{D} \quad (5)$$

where

C_g = Capacitance to ground plane in pF
 ϵ = relative dielectric constant

Thus, the thinner the substrate, the greater the film capacitance to ground. If we now solve (2) for P , the power dissipated in the film, and take the ratio of dissipated power to capacitance, we get

$$\frac{P}{C_g} = 0.113 \Delta T \frac{k}{\epsilon} \quad (6)$$

This tells us that, for a given temperature rise limit, ΔT , the ratio of dissipated power to capacitance is a constant, dependent only on two physical properties of the substrate material, and not on the substrate thickness or film area. Stated alternately, **Power handling is directly proportional to capacitance to ground.** Since, as will be shown below, capacitance fundamentally limits electrical performance, the quantity $M = \frac{k}{\epsilon}$ from (6) may be taken as a figure of merit of a substrate. Using the values of Table 1 at 200 °C, $M_{BeO} = 22.4$, $M_{AlN} = 13.9$, and $M_{BeO}/M_{AlN} = 1.6$. Thus, beryllia would always be the substrate of choice over aluminum nitride – were it not for the former's toxicity.

Note that (6) may be re-written as:

$$R_{TH} C_g = 8.85 \frac{\epsilon}{k}, \quad \text{where the thermal resistance, } R_{TH} = \frac{\Delta T}{P} \quad (7)$$

Thus, the product of the chip's thermal resistance and electrical capacitance to ground is a constant inversely proportional to the substrate figure of merit.

Capacitance-to-ground vs. termination input reflection

We may now examine the effect of capacitance on electrical performance. This is perhaps done most readily using a termination as an example. We begin by deriving an equivalent circuit for a shorted section of lossy line. This given by,

$$Y_{IN} = Y_0 \coth \gamma l, \quad \text{where } l \text{ is the line length and } Y_0, \text{ the characteristic admittance, is:} \quad (8a)$$

$$Y_0 = \sqrt{\frac{G + j\omega C}{R + j\omega L}} \quad \text{and } \gamma, \text{ the propagation constant, is} \quad (8b)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (8c)$$

R, **L**, **G**, and **C** are respectively the resistance, inductance, conductance, and capacitance per unit length; ω is the angular frequency = $2\pi f$. For a low-loss substrate such as AlN, G can generally be neglected compared to ωC . To obtain a lumped equivalent circuit for the shorted transmission line, we use a power series expansion for $\coth x = 1/x + x/3 - x^3/45 + \dots$, where $|x| < \pi$. Then, taking the first two terms of the series, (8a) becomes:

$$Y_{in} = \left(\frac{j\omega C}{R + j\omega L} \right)^{0.5} \left[\frac{1}{[(R + j\omega L)(j\omega C)]^{0.5}} + \frac{[(R + j\omega L)(j\omega C)]^{0.5}}{3} \right] = \frac{1}{(R + j\omega L)} + \frac{j\omega C l}{3} \quad (9)$$

We recognize this as the admittance of the circuit shown in **Figure 9**. The inductance and capacitance both impose limits on how well matched we can make the termination over a given bandwidth.

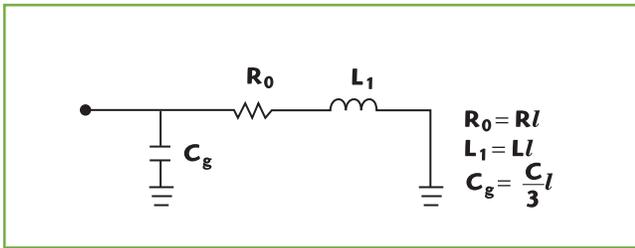


Figure 9: Low frequency lumped equivalent circuit for short-circuited lossy line

In the late 1940's, H.W. Bode considered the problem of impedance matching two-element RC or RL loads.³ Bode's work was extended and generalized by Fano in 1950; Fano presented the limitations on impedance matching *any* load over an angular frequency range, ω_a to ω_b . However, for illustrative purposes, let us consider the case analyzed by Bode, i.e., where the inductive reactance is so much less than the value of the resistance at the highest frequency of interest that we can neglect the inductance altogether. For further simplicity, we take the lower frequency as zero (DC). Then, applying Bode's formula to the circuit of Fig. 9, the best possible results are limited as indicated by

$$\int_0^{\omega_b} \ln \left| \frac{1}{\Gamma} \right| d\omega = \frac{3\pi}{R_0 C_g} \quad (10)$$

Or, in words, the area under the curve of $\ln \left| \frac{1}{\Gamma} \right|$ vs. ω can be no greater than $\frac{3\pi}{R_0 C_g}$.

Substituting from (6),

$$\int_0^{\omega_b} \ln \left| \frac{1}{\Gamma} \right| d\omega = \frac{1.06 \Delta T k}{R_0 P \epsilon} \quad (11)$$

Equation (11) describes the best tradeoff that can be achieved between power handling and area under the curve of $\ln |1/\Gamma|$ vs. ω . For a given permissible film temperature rise: The higher the applied power, the less the area under the curve. If $|\Gamma|$ is assumed constant over the band,

$$|\Gamma| = e^{-\frac{0.169 \Delta T k}{f_b R_0 P \epsilon}} \quad (12)$$

from DC through f_b , and unity everywhere else.

It is seen that: (a) **The higher the (applied) power-bandwidth product, the higher the minimum achievable reflection for a given film temperature rise;** and (b) **The higher the figure of substrate merit $M = k/\epsilon$, the lower the reflection magnitude.**

Note that (12) is a theoretical result that can be achieved only with an infinite number of matching elements. Real-world chips are subject to many additional limitations including (but not limited to) having: (a) space for only one or at most two matching elements; (b) inductances non-negligible compared to the terminating resistance; (c) lengths that are not electrically short at operating frequencies; (d) tolerances on dielectric constant, thermal conductivity, and physical dimensions of matching elements; (e) film dimensions that require trimming to bring them into resistance specification; and (f) protective cover films and ceramic lids that add parasitic reactances. Thus, the reflection magnitude over a given frequency band will be substantially higher than indicated by (12), but the qualitative dependencies still apply.

POWER RATING: DEFINITION AND CONFIRMATION

Before we can do a thermal design, we must first decide on exactly what we shall mean by "power rating" for a chip device. **Figure 10** illustrates the heat flow around a mounted chip resistor. The resistive film, assumed to have constant power dissipation over its surface, behaves as an isoflux boundary, i.e., a source of uniform heat flux, rather than the isothermal boundary used in the derivation of equation (2). Were the film to completely cover the chip, the isoflux case would approach the isothermal case, but absent that condition the heat spreads out as shown.

The thermal resistance between two points is defined as the temperature difference between those points divided by the heat flow (typical units are degrees Centigrade/Watt). It is analogous to electrical resistance, with temperature corresponding to voltage and heat flux to current. **Figure 10** indicates that there is vertical as well as lateral heat flow in both the ceramic chip and the carrier it is mounted on. This implies that the system must be represented as a lattice network of thermal resistances rather than a single

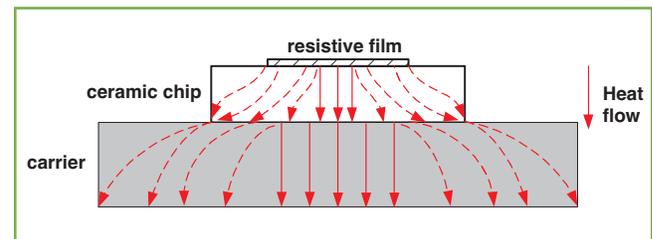


Figure 10. Heat flow around a mounted chip resistor

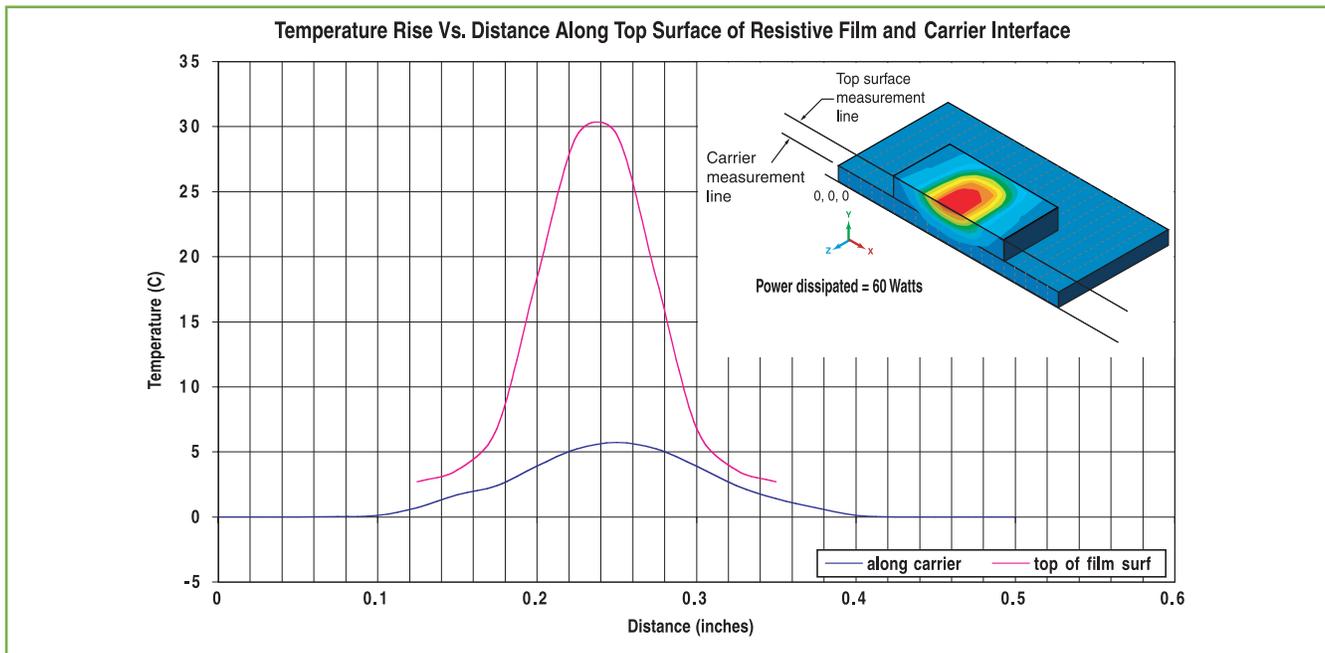


Figure 11: Computer simulation of isotherms around mounted chip resistor

thermal resistance. (The latter can characterize only the kind of one-dimensional heat flow assumed for equation (2)) **Stated alternately, the temperature will vary laterally along the film and, also, laterally along the mounting surface.** This is illustrated in Figure 11, which was made using a "Finite Element Method" (FEM) computer simulation. In actuality, a three-dimensional latticework of resistors is needed to describe a mounted resistive chip, and there is temperature variation along all three dimensions.

The above considerations bear importantly on how a chip is designed and characterized for power handling and exactly how confirming measurements are made. Figure 12 indicates temperatures at a number of points on and around a mounted chip: (a) T_0 , at the film centroid; (b) T_1 , at the film edge or corner; (c) T_3 , on the mounting surface directly under the film centroid; and (d) T_2 , on the mounting surface 30 mils away from the chip edge. We can make the following qualitative observations:

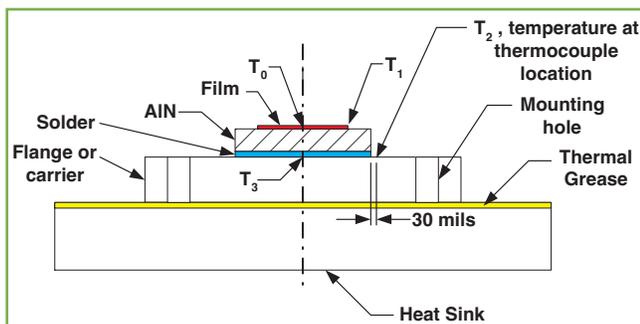


Figure 12: Temperatures at a number of points on and around a groundplane-mounted resistive chip

- Thermal aging will likely depend on the area-averaged temperature over the film. The peak temperature has no particular significance – unless it is sufficiently extreme to cause catastrophic failure.
- T_0 is the temperature at the nominally hottest point on a film disposed symmetrically on a chip – which is the case for resis-

tors, but not terminations. The actual (as opposed to nominal) hottest film point may be at a fault location – where the film was laser-trimmed, where there was a thin spot or substrate pull-out, at the interface to the conductive contact – and can only be determined experimentally.

- Instruments without sufficient resolution, e.g., a thermal camera with a 30-mil diameter spot size, may not be able to accurately measure T_0 or any other hot spot, especially on large films where the temperature is changing rapidly across the surface.

An ideal heat sink has infinite thermal conductivity and, because of this, the infinite thermal conductivity, T_2 would equal T_3 in Fig. 12. From Fig. 10 and Fig. 11, this clearly is not the case for any real mounting surface; in fact, $T_3 > T_2$.

One strategy for defining power rating might be to measure T_3 directly – or deduce it from a measurement of T_2 and a computer FEM model – and then specify performance as if an ideal heat sink were held everywhere at that temperature. By slicing a mounted resistor in half along its longitudinal axis – in Figure 12, perpendicular to the plane of the paper, down the centerline – we were able to take advantage of the lateral heat-flow symmetry to measure T_2 and T_3 for chips of several sizes and input powers. (The slice plane is an adiabatic boundary, i.e., no heat flows across it.) Results of such measurements are presented in Table 2. All chips were 40 mils thick and all measurements were made on a silver-plated high-conductivity copper mounting surface (see the table for more information).

TABLE 2: Temperature difference between two points on mounting surface of sliced resistive chips

Chip		Film		Power Applied (Watts)	$T_3 - T_2$ (°C)
Length (mils)	Width (mils)	Length (mils)	Width (mils)		
200	100	146	84	30	5.7
250	250	196	112	60	12.9
375	250	321	184	150	15.3

Although measurements of the type made above can be performed in a laboratory environment, this approach is not practical for mass-production testing. Thermal modeling presents an equal number of practical problems, not the least of which is the considerable uncertainty in the material constants (thermal conductivity of AlN, solder, heat sink) for any particular mounted chip. Further, in either case – and perhaps most importantly – the results would be difficult, tedious, or impossible for end-users to confirm; in most cases, they would have to "take our word for it," hardly an enviable position. Instead, ATC has decided on a set of defined measurement conditions that are readily reproducible and that yield verifiable results. The resulting power rating, of course, is lower than it would be on an ideal heat sink.

How we specify power rating

- First, we must define the chip mounting conditions: **Our tests are conducted on large (1.2-inch x 1.05-inch, 0.188-inch thick) silver plated C110 copper alloy carriers.**
- Next, since our carrier does not have infinite thermal conductivity, we must specify the **exact location – T_2 in Figure 12 – at which we hold the ambient temperature constant. Typically, we choose this as 30 mils from the chip edge along its lateral centerline** – an arbitrary, convenient spot at which to solder a small thermocouple.
- Finally, we specify the measuring instrument: **Temperature measurements are made with a contacting fiber-optic thermometer – Luxtron Model 790** – that does not depend on emissivity for accuracy and that has a measurement spot size on the order of 10 mils. in diameter.

Having specified the measurement conditions we are now ready to declare how we establish the power rating of a given device:

With rated power applied and location T_2 on the standard carrier held at a specified ambient temperature, two conditions shall be met: (1) The first, termed "power handling," is that maximum film temperature shall not exceed a specified value; (2) The second, termed "life," is that the film resistance change no more than a specified percentage during and after a 1000-hour burn-in per Mil-PRF-55342. Typical values of parameters are: ambient temperature = 100 °C; maximum spot film temperature = 170 °C; percentage resistance change \leq 0.2%.

Having at last come to a definition of power rating, actual designs can now be implemented.

THE DESIGN PROCESS

Resistors

The design process for resistors is relatively straightforward. Various chip sizes have become standardized in the industry, e.g., 0.200" x 0.100", 0.250 x 0.250, etc. Chip thicknesses have become equally standardized; the three most common are 25, 40, and 60 mils. Contact lengths are determined by mechanical constraints: exposed bonding areas – leaving room for film coating overlap – needed to insure that tabs have sufficient pull strength. In general, contact widths should be about the same as the film width; the contacts are parasitic, that is, they contribute to capacitance (and inductance) without dissipating any heat. With the length of the film now determined – chip length minus contact length – the width is chosen to yield an area in accordance with the peak temperature and aging requirements.

There is, however, one complication: Be the implementation thick-film or thin-film, there is always a spread of resistance values about any given nominal target. In thin-film, a total spread might be 15%,

i.e., if a target resistance were 100 ohms, actual resistor values might vary from 85 to 100 ohms. For safety in design, a spread of 20% is typically allowed. Since resistors are often sold to $\pm 2\%$ or tighter tolerances, in general, trimming will always be required. While low-power resistors are often trimmed by cutting notches perpendicular to the length dimension, current concentrations along the edges of such notches can result in local hot-spots. The result would be burn-out at high power RF inputs. Instead, ATC laser-trims resistors by narrowing the width dimension symmetrically and uniformly along the length. Thus, any design must accommodate width dimensions that vary over a 20% range; i.e., a resistor trimmed to the maximum extent must still meet all thermal and electrical requirements.

In order of increasing accuracy (and decreasing convenience), film temperatures can be estimated by: equation (2) herein (no spreading); any one of several formulas available in the literature that include spreading; or an FEM computer program. The term "constriction resistance" is used to describe that component of thermal resistance over and above what would be produced by purely one-dimensional heat flow. Let us assume a perfectly conducting mounting surface in Figure 10, i.e., a surface along which there can be no lateral temperature variation. Then to calculate the total thermal resistance from the film to the mounting surface, one would compute the one-dimensional resistance of the chip with the film occupying its entire surface and then add the constriction resistance to account for the lateral constriction of the heat-flow. (Note, from the top down the heat spreads and so the term "spreading resistance" is frequently used, but from the bottom up the heat flow constricts.) There are several expressions available in the literature for the constriction resistance of heat sources mounted on rectangular channels ("flux tubes") with adiabatic walls, i.e., heat-producing films on chips that have no appreciable heat conduction perpendicular to their sidewalls. One formula that yields constriction resistance based on an average film temperature is⁵.

$$\Psi = 0.475 - 0.62\varepsilon + 0.13\varepsilon^3 \quad (13)$$

Where $\Psi = \sqrt[3]{R_C R_c}$, a dimensionless spreading resistance

R_C = spreading resistance

k = thermal conductivity

A_f = area of film

ε = square root of ratio of film area to chip area

The problem with any of the above methodologies is that it is quite difficult to accurately match experimental results with their predictions. The principal reasons are uncertainties in the experimental data: the exact thermal conductivity of the particular substrate being measured and its variation with temperature, the exact thermal conductivity of the carrier, the integrity of the solder joint between chip and carrier (see more about this later), the exact positions of temperature measuring devices, etc. Thus, insofar as initial design efforts, methodologies beyond one-dimensional calculations are of marginal utility. Of course, other insights that they provide, both qualitative and quantitative, as well as tolerance study capabilities, may justify the extra time and effort.

Capacitance to ground can be calculated, again in order of increasing accuracy, using: (5) herein (no fringing); formulas available in the literature for microstrip impedance (includes electric field fringing, but not substrate truncation); or an Electromagnetic (EM) analysis program such as Sonnet or Eagleware. The second alternative deserves some elaboration. The standard formulas for

the impedance of microstrip line assume an infinitely wide substrate. A resistive chip, however, is fabricated as a substrate that is **truncated** at a certain distance from the edge of the trace. Thus, standard microstrip impedance formulas could be in considerable error for resistive films whose lateral edges approach the edges of the substrate. In general, if the trace-edge-to-substrate-edge is greater than half the trace width, impedance values will be affected by < 0.5%.⁶ Standard formulas for microstrip characteristic impedance, Z_{OM} , and group velocity, v , are widely available. The total capacitance to ground of the chip is then given by

$$C = (l + 2l_c) \frac{1}{Z_{OM}v} \quad (14)$$

where l = length of film
 l_c = length of contact (assumed same width as film)

The equivalent circuit for a resistor may be derived by considering it as a length of lossy line. The admittance matrix for such a section is given by⁷

$$[Y] = \begin{bmatrix} \frac{\coth \gamma l}{Z_0} & \frac{-1}{Z_0 \sinh \gamma l} \\ \frac{-1}{Z_0 \sinh \gamma l} & \frac{\coth \gamma l}{Z_0} \end{bmatrix} \quad (15)$$

The pi-equivalent is shown in **Figure 13a**; when the electrical length, γl , becomes short and the approximations $\tanh \gamma l = \sinh \gamma l = \gamma l$ apply, the series impedance is given by

$$Z_{0\gamma l} = 1 \sqrt{\frac{R + j\omega L}{G + j\omega C}} \cdot \sqrt{(R + j\omega L)(G + j\omega C)} = (R + j\omega L) l \quad (16)$$

while the shunt impedances are given by

$$\frac{Z_0}{\gamma l} = \frac{2 \sqrt{\frac{R + j\omega L}{G + j\omega C}}}{1 \sqrt{(R + j\omega L)(G + j\omega C)}} = \frac{1}{\frac{Gl}{2} + \frac{j\omega Cl}{2}} \quad (17)$$

The equivalent circuit then becomes that shown in **Figure 13b**. (We neglect, as earlier, G compared to ωC .) Note that the circuit contains both inductance and capacitance parasitics, though most vendors electrically characterize a chip resistor only by the latter. C_1' is then given by half the value calculated in (14), while L_1' is given by

$$L_1' = (1 + 2l_c) \frac{Z_{OM}}{v} \quad (18)$$

Note that to calculate the thermal and electrical effects of a protective coating and/or ceramic cover, only an FEM thermal program and an EM electrical program can do the job.

Terminations

Termination design begins analogously to resistor design – input contact length and edge-wrap-to-ground length must first be

subtracted from the chip length to determine the available working space. But the latter now has two required functions: to support a means of heat dissipation (i.e., resistive film) and to support an impedance-matching network. The resistive film must then meet the following criteria:

- Satisfy the peak temperature and aging requirements
- Have an input impedance that can be readily matched by a simple one- or two-reactance network
- Leave sufficient room for implementation of the matching network

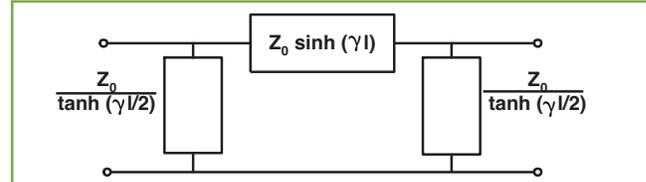


Figure 13a: Pi-equivalent circuit of lossy line

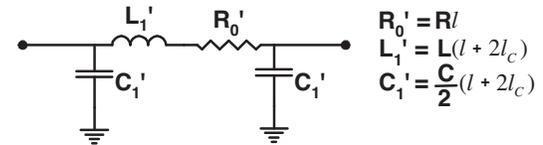


Figure 13b: Equivalent circuit of chip resistor

The interplay among (a), (b), and (c) above must usually be done utilizing a number of iterative back-and-forth trials with both thermal and electrical CAD programs. The chip layout – a truncated dielectric, protective coating, and (in some cases) ceramic cover – containing matching elements that couple to each other and have large discontinuities, gives rise to impedances that cannot be accurately modeled with circuit-based programs (e.g., Touchstone) alone. Similarly, the thermal behavior of the non-centered film plus wraparound cannot be accurately described by closed-form spreading equations (e.g., (13) herein). Therefore, CAD suites must be used for both aspects of design.

Typically, the length-to-width (aspect) ratio of the film is chosen so that its input impedance can be incorporated into a low-pass filter structure. **Figure 14** shows the equivalent circuit of a film plus matching network. The element immediately preceding the film, L_2 , is an inductor, generally realized by an electrically short (but often physically meandered) length of narrow (high-impedance) line. (Note that a strength of thin-film implementation is that the tolerance on the line width, and hence its impedance, can be controlled very tightly; the result is an improved VSWR yield compared to a thick-film design.) The input element, C_2 , which incorporates the contact, is a shunt capacitor.

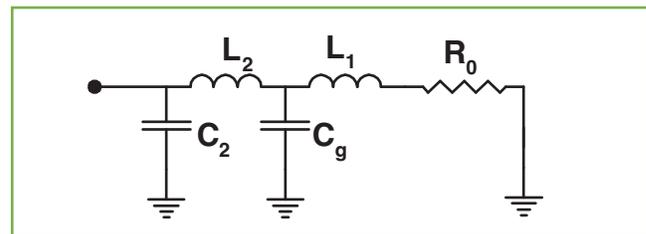


Figure 14: Equivalent circuit for matched termination

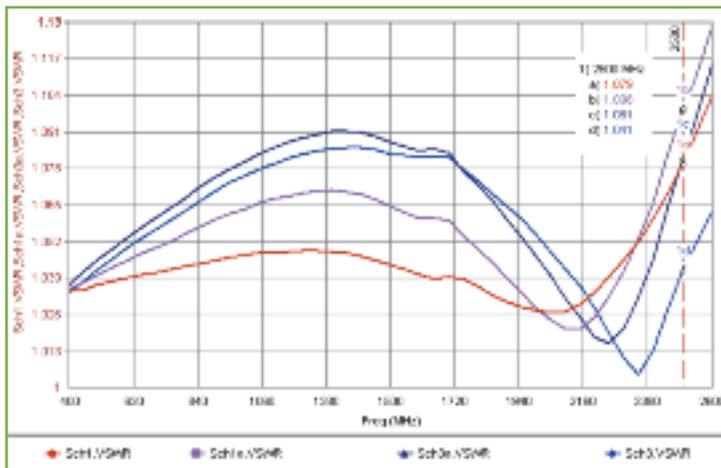
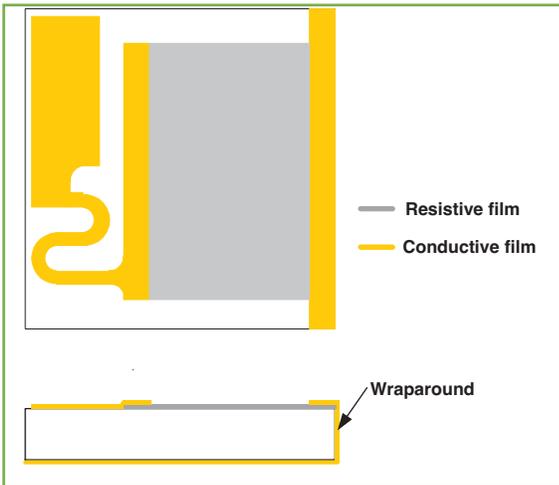


Figure 15: Physical layout of 60-Watt termination

Figure 16: VSWR of 60-Watt termination

As with resistors, any design must accommodate a film width variation of 20%, as well as the specified range of AlN dielectric constant, which typically varies from 8.7 to 9.3. These two factors, plus variation of all physical dimensions and substrate and cover dielectric constants all affect production yield to a given VSWR. Figure 15 shows the physical layout of a 60-watt chip termination; Figure 16 shows typical VSWR-vs.-frequency plots

of 60-watt terminations randomly selected from a production run. Figure 17 shows thermal scans made using an IR camera with the termination at full rated power and the mounting surface temperature at 100 °C, when measured at a point 30 mils from the termination edge (as described in the section herein titled, **How we specify power rating**).

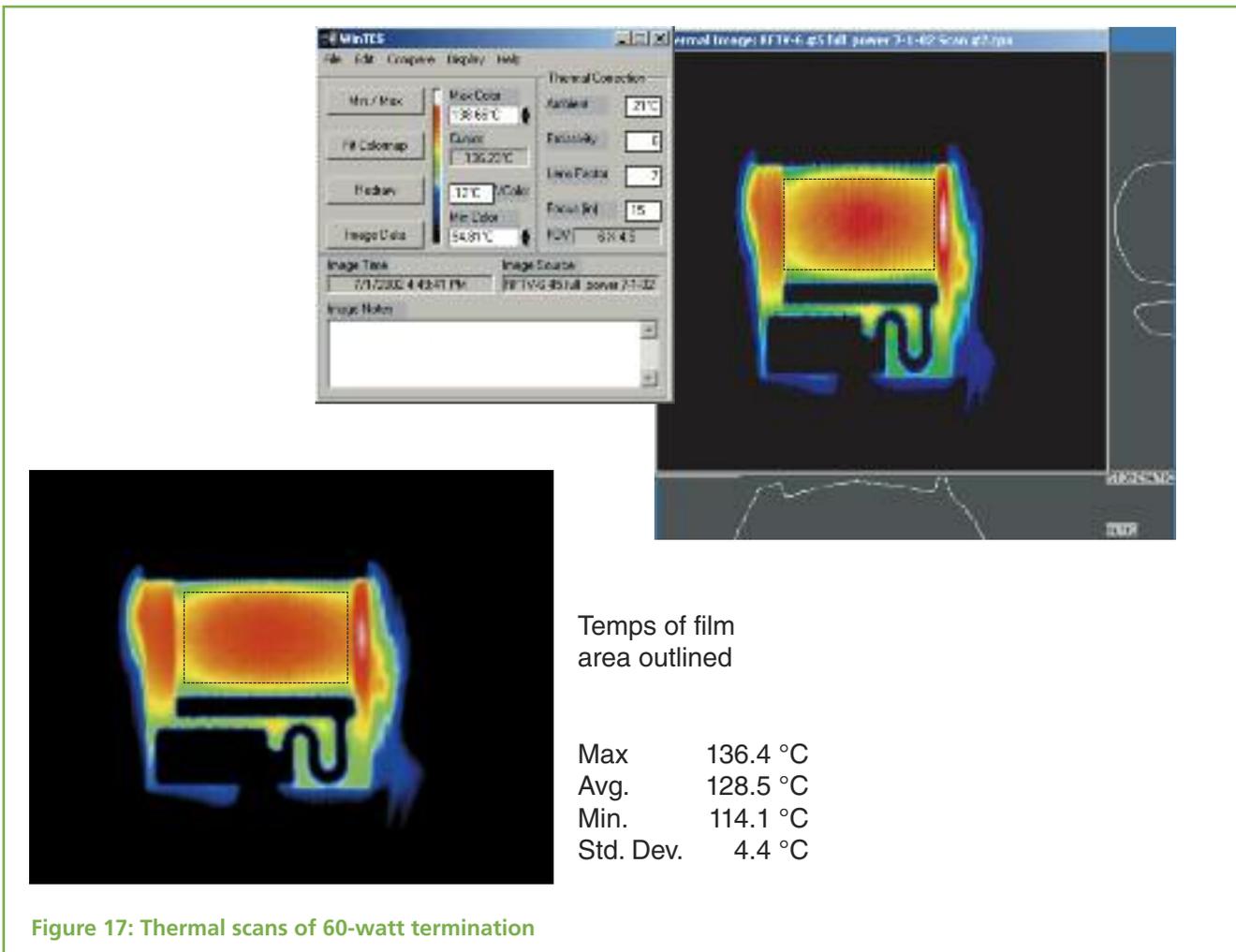


Figure 17: Thermal scans of 60-watt termination

It was discussed under (10) and (11) that the area under the $\ln \left| \frac{1}{\Gamma} \right|$ vs. frequency curve is a constant. Thus, better match at any particular frequency is always achieved at the expense of match at another frequency. **If a termination VSWR is specified from DC to an upper frequency value, as is typical practice, optimum designs are mismatched at DC so that improved match can be achieved across the entire band. ATC follows this design practice, so users should be aware that, for instance, a DC measurement of a 50-ohm termination will not necessarily be exactly 50 ohms.**

How we measure reflection

It was alluded to earlier that reflection measurements are subject to a number of vagueries that include not only the interface to the measuring equipment – test board thicker or thinner than termination substrate, trace wider or narrower than the termination tab, board dielectric constant – but also the details of the measurement technique. **ATC measures termination reflection under the following conditions:**

- **Test substrate is Rogers Corp. TMM3, dielectric constant = 3.27**
- **Board thickness = chip substrate thickness = 40 mils, nominal**
- **Board trace width = 92 mils (for $Z_0 = 50$ ohm line)**
- **Measuring instrument is an Agilent 8722D Vector Network analyzer with a 4-receiver architecture**
- **Measurement is performed using standard TRL de-embedding to remove the effects of connectors and source-load-UUT mismatch interactions**
- **Termination front surface is butted against TMM test board, no strain relief in tab**
- **Tab length = 90 mils.**

VIA PATCHES FOR SURFACE-MOUNT COMPONENTS

As shown in Figure 3b, surface mount (SMT) parts are typically soldered to a via patch in order to transfer the heat generated in the resistive film to a ground plane/heat sink. The question of how to rate an SMT part for power handling is thus intimately connected with the via patch it is to be mounted on. Among the variables in via patch design are board thickness, and via hole diameter, via hole spacing, via hole pattern, via hole plating, and via hole solder filling. Each end-user will typically have its own preferred set of the above parameters. In an effort to characterize SMT device performance, ATC has adopted a standard via patch design and test methodology that provides sufficient information for end-users to calculate behavior in their own operating environments. The design assumptions and parameters of ATC's standard via patches are presented below.

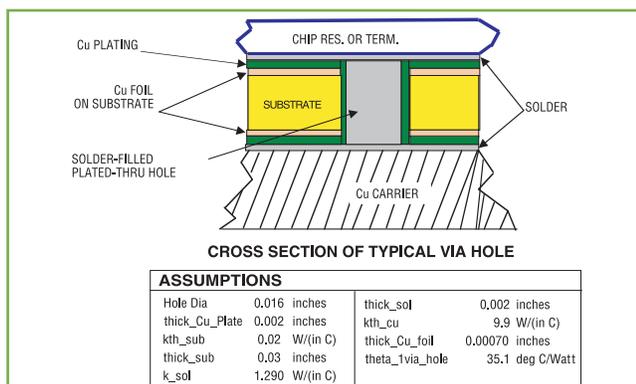


Figure 18: Via-hole cross section and parameters

PC board: Rogers Corp. 4350; 30 mils thick; 1/2-oz. (7 mils thick) copper cladding.

Via holes: See Figure 18. Structure – plated through with 2-mil copper, filled with Sn 63 solder; Diameter = 16 mils; edge-to-edge spacing = 0.5 x diameter = 8 mils. Notes – The minimum via hole diameter is generally a function of board thickness and is related to "walking" or breaking of the drill bit. The maximum via hole diameter relates to the ability to wick up solder to the via's full length. Different PC board fabricators will have different design rules that apply.

Pattern: Rectangular array. Notes – There are two possible uniform patterns, designated *Rectangular Array* and *Triangular Array* respectively, and shown in Figure 19. For optimum design, it must be determined which pattern places the most via holes under a chip. This consideration can become fairly complex, since vias that are even partially under a chip can still contribute significantly to heat conduction. Although details are beyond the scope of this discussion, ATC has developed some useful algorithms to aid in optimum via-patch design; customer assistance is available from the factory. For most – but not all – situations, the rectangular array yields better results than its triangular counterpart.

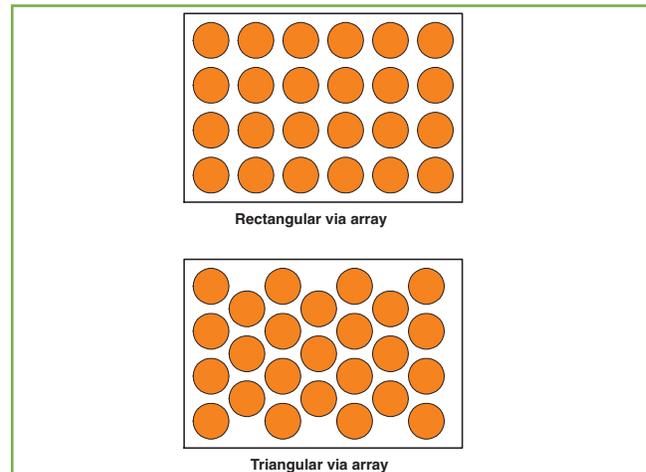


Figure 19: Rectangular and Triangular via arrays

The calculated thermal resistance of each via, with the assumptions above, is 35 °C/Watt. Table 3 and Table 4 below present calculated performance parameters of ATC's standard via patches for various sizes of CS-style SMT chip resistors and CZ-style SMT chip terminations (see Figure 4 for style diagrams).

Table 3: Calculated Via-Patch Performance for CZ-Style Terminations Assumptions:

1. No lateral heat transfer on surface.
2. Board is solder attached to an ideal heat sink.
3. Thermal resistance of each via is 35 °C/Watt

Chip Type CZ	Rated Power of Chip (Watts)	Number of Vias	Thermal Resistance of Board (°C/Watt)	Temperature drop across board at rated Power (°C)
0.200 × 0.100	10	30	1.17	11.7
0.250 × 0.250	20	88	0.40	8.0
0.375 × 0.250	30	132	0.27	8.1
0.375 × 0.375	40	204	0.17	6.9

Table 4: Calculated Via-Patch Performance for CS-Style Resistors

Assumptions:

1. No lateral heat transfer on surface of board.
2. Board is solder attached to an ideal heat sink.
3. Thermal resistance of each via is 35 degrees C/Watt

Chip Type CS Size (L x W)	Rated Power of Chip (Watts)	Number of Vias	Thermal Resistance of Board (°C/Watt)	Temperature drop across board at rated Power (°C)
0.200 × 0.100	10	20	1.75	17.5
0.250 × 0.250	20	48	0.73	14.6
0.375 × 0.250	30	96	0.36	10.8
0.375 × 0.375	40	144	0.24	9.7

An example of via patch tests were those run on four CS 2010 resistor chips. The chips were first mounted directly on modified standard large copper carriers. (The chips actually sat atop a small ridge so that their bottom sides would not be short circuited). Referring to Figure 12, with carrier temperature T_2 at 100 °C, 10 Watts DC was applied to the chip, and the resultant peak film temperature rise, $T_0 - T_2$, was measured at 15.4 °C (average for the 4 chips). Thus, the chip peak thermal resistance measured as $15.4/10 = 1.54$ °C/Watt. Next, the same type chips were mounted on a standard (as designed above) via patch board – see Figure 20 – which was soldered to a carrier. With T_2 – now measured on the via patch – held at 100 °C, the peak film temperature rise was 34.7 °C.

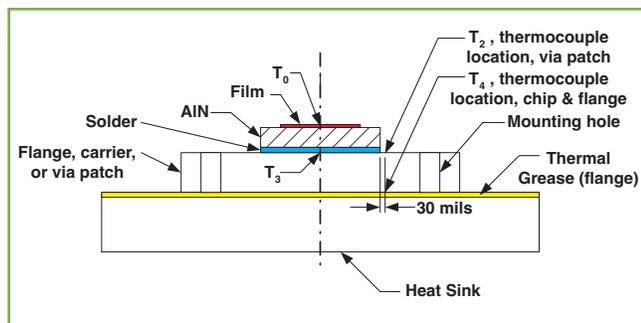


Figure 20: Temperatures at a number of points on and around a flange- or surface-mounted resistive chip

A second experiment was done in which, with the via patch in place, the carrier temperature T_4 directly under point T_2 was held at 100 °C. The measured resultant $T_0 - T_2$ was 34.5 °C. We can compare this to the predicted value by adding the chip thermal resistance, 1.54 °C/Watt, to the via thermal resistance (from Table 4), 1.75 °C/Watt, and multiplying by 10 Watts. The result, 32.9 °C, compares reasonably well with the measurement.

How we specify power rating on SMT parts

The power rating of an SMT part, mounted on the standard via patch, is specified in the same way as for non-surface mounted parts – see herein under How we specify power rating – except that location T_2 , the point held at the specified ambient temperature, is on the surface of the via patch.

Note that we could have equally well required T_2 to be on the carrier instead of atop the via patch, but the latter location seems more practical, in that it is a point users can readily measure and control through their own heat sink and via patch design.

FLANGE MOUNTED PARTS

The power rating of flange-mounted chips presents problems similar to those of SMT chips. In general, flanges are not particularly good conveyers of film-generated heat to the mounting surface. The interface is characterized by several factors:

- a) Intimate contact occurs at discrete parts of the nominal interface
- b) A very thin gap exists in the regions where there is no intimate contact, and is usually occupied by a third substance, e.g. air, other gasses, grease, or other material
- c) Heat transfer can take place by conduction through the real contact area, by conduction through the substance in the gap, and by radiation across the gap.

The actual thermal resistance of an interface depends on surface roughness, waviness and slope of the contacting peaks; thickness of the non-contact region; type of interstitial fluid (gas, liquid, grease, vacuum); interstitial gas pressure; thermal conductivities of the contacting solids and interstitial substance; hardness or flow pressure of the contacting peaks (plastic deformation of the highest peaks of the softer solid); modulus of elasticity of the contacting solids (elastic deformation of the wavy parts of the interface); and average temperature of the interface (radiation and property effects). Thus, thermal contact resistance is an extremely complex problem – which makes characterization and measurement of products whose performance depends on such an interface equally complex.

Using pressure-sensitive indicating tape, ATC has determined that for a flange that is simply bolted to a mounting surface there is reliable contact only over the area of the mounting hole plus a small surrounding annulus. Thus, a substantial portion of the heat generated by the chip proceeds in a lateral direction through the flange until it gets to the vicinity of the mounting hole, whence it is redirected vertically through the mounting bolt to the heat sink. Thermal grease does permit vertical heat flow over the entire flange, but even the best thermal greases have thermal conductivities far less than metals and are messy to apply and remove. If using thermal grease, it is important to control the average thickness; this is best done by controlling the volume and using a spatula or roller to evenly distribute it over the flange surface area. A maximum 2-mil thickness of grease is recommended.

One-hole flange

An example of flanged-part tests were those run on four FR10515 resistors. When chips of the type used for this part are soldered directly on standard large silver-plated copper carriers (surface finish after plating = 10-15 µin., avg.) and T_4 (see Figure 20) is held at 100 °C, the peak film temperature rise, $T_0 - T_4$, is typically 35.6 °C at the rated 45-watt input power. When the same type chips are mounted on single-hole flanges, bolted down – without thermal grease – to the carriers at the recommended torque, the carrier (point T_4 , Fig. 20) held at 100 °C, and the same 45-watts input power applied, the peak film temperature rise increases to 70 °C.

When an AIN-based thermal grease (AiT COOL-GREASE™ CGR 7018) was applied such that an approximately 2-mil thickness resulted between the flange and mounting surface and the above test was repeated, the peak film temperature rise was only 49 °C.

Two-hole flange

An example of two-hole flange tests were those run on four FR10870 resistors. When chips of the type used for this part are soldered directly on standard large silver-plated copper carriers (surface finish after plating = 10-15 μm , avg.) and T_4 (see Figure 20) is held at 100 °C, the peak film temperature rise, $T_0 - T_4$, is typically 66 °C at the rated 150-watt input power. When similar chips are mounted on two-hole flanges, bolted down – without thermal grease – to the carriers at the recommended torque, and the carrier (point T_4) held at 100 °C, a 66 °C temperature rise occurs for an applied power of only 106 watts. (Note that to measure the carrier temperature, a small hole was drilled in the flange at the T_2 - T_4 location and the Luxtron fiber optic probe inserted in the hole until it contacted the carrier.)

When an AlN-based thermal grease (AiT COOL-GREASE™ CGR 7018) was applied such that an approximately 2-mil thickness resulted between the flange and mounting surface and the above test was repeated, the 66 °C peak film temperature rise occurred at an applied power of 120 watts.

How we specify power rating of flange-mounted devices

The power rating of a flanged part is specified in the same way as for chips – see herein under **How we specify power rating**. Location T_4 , the point held at the specified ambient temperature, is on the surface of the carrier. Note that some vendors specify ambient temperature as T_2 on the top surface of the flange instead of T_4 on the carrier or heat sink. This will produce an apparently higher power rating, since the thermal drop through the flange is not accounted for in the measurement. ATC believes that end users can most readily control the temperature of the flange mounting surface rather than the flange top surface, and thus we specify the power capacity appropriately.

SOME RECOMMENDATIONS ON SOLDERING

When mounting chips, the solder interface to the mounting surface has a crucial bearing on performance. Even with careful soldering technique, voids (porosity) and de-wetting are difficult to avoid. Using Scanning Acoustic Microscopy (SAM), radiographic analysis, and metallographic sectioning, ATC has studied solder joints made with a variety of techniques. **One result is that, where typical surface mount assembly techniques are used, such as those involving solder paste, porosity levels of 10 – 25% should be expected.** Note that this directly transfers to the power rating of the part, i.e., its power handling capability will decrease in approximately the same proportion.

Here are some suggestions to improve solder joint integrity:

Avoid the use of hold-down clamps or springs. Loading the solder in compression during melting forces it out of the bond area and does not permit the "Z" direction movement required during solidification to reduce shrinkage porosity. Further, the thermal mass of the hold-down fixture may cause a lag in temperature, resulting in a cooler part and loss of solder in the bond area when the chip eventually reaches the correct temperature.

Avoid introducing solder to the entire bond area prior to soldering, i.e., do not use a solder pre-form the same size as the entire resistor chip or pre-tin the entire chip bottom. **Porosity reduction is enhanced by permitting the solder to wick through the joint area by capillary action, preferably from a central location.**

Reduce the soldering time (temperature above solder melting point) to 20-30 seconds maximum in order to avoid scavenging of the silver plating, intermetallic formations, solder melting point alteration, etc.

Reasonably good results have been achieved at ATC using lengths of solid Sn96 (Sn96.5/Ag3.5) wire, about 0.030 inches in diameter, placed in the center of the chip, with RMA flux applied to both chip and mounting surface. This process has been shown to result in porosity levels of 8-12%; optimized solder volumes may yield even better results.

CONCLUSIONS

Both vendors and end-users of high-power microwave resistive chip products are frequently guilty of a lack of rigor in specification. A likely reason is that many of these products see use only during fault conditions. After all, apart from microwave ovens and dryers, no one wants to spend a great deal of time turning microwaves into heat. Thus, unlike transistors, capacitors, or inductors, resistive parts that under-perform (or even fail) may go undetected without catastrophic results – much of the time. However, by understanding actual measurement conditions and fundamental physical constraints, users can often save the added cost of an over-designed part as well as insure themselves of a more reliable product during those crucial intervals when it is in use.

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